# DIGITAL COMMUNICATIONS

Analog and digital modulation systems use analog carriers to transmission of information. However, with analog modulation systems, the information signal is also analog, whereas with digital modulation, the information signal is digital

There are four types of digital modulation systems-

- Amplitude Shift Keying (ASK)
- Frequency Shift Keying (FSK)
- Phase Shift Keying (PSK)
- Quadrature Amplitude Modulation (QAM)

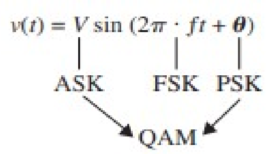
ASK is a type of Amplitude Modulation which represents the binary data in the form of variations in the amplitude of a signal.

FSK is the digital modulation technique in which the frequency 'f ' of the carrier signal varies according to the changes in the digital signal.

PSK is the digital modulation technique in which the phase (θ) of the carrier signal is changed by varying the sine and cosine inputs at a particular time.

QAM is the digital modulation technique in which the amplitude and the phase are varied proportional to the information.

This is represented in the following equation.




**Applications of Digital modulation:**

DIGITAL COMMUNICATIONS are used in -

(1) Relatively low-speed voice-band data communications modems
(2) High-speed data transmission systems
(3) Digital microwave and satellite communications systems and
(4) Cellular telephone Personal Communications Systems (PCS).

**Block Diagram Of Digital Modulation System**

The simplified block diagram for a digital modulation system as shown below.

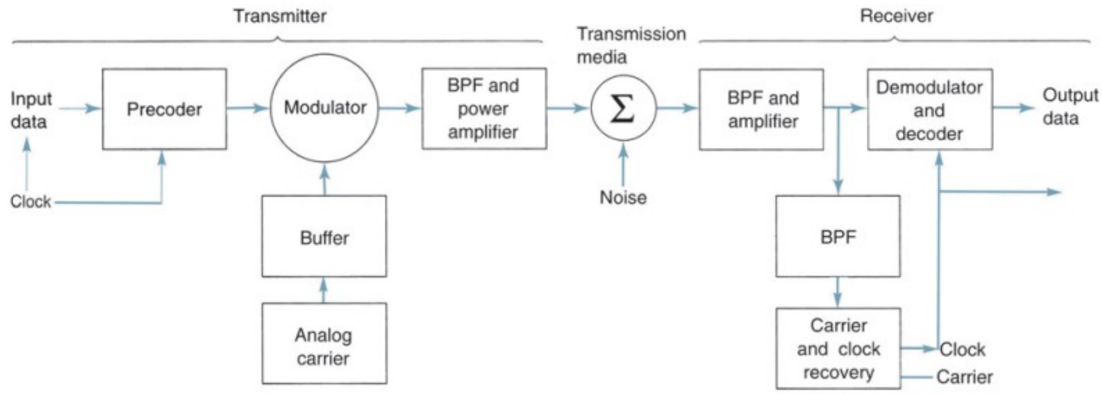



FIGURE 1 Simplified block diagram of a digital radio system

The modulation system has two sections-

- Transmitter and
- Receiver.

**Transmitter:**

In the transmitter, the precoder performs level conversion and encodes the incoming data into groups of bits that modulate an analog carrier. The modulated carrier is shaped (filtered), amplified, and then transmitted through the transmission medium to the receiver. The transmission medium can be a metallic cable, optical fiber cable, Earth's atmosphere, or a combination of two or more types of transmission systems.

**Receiver:**

In the receiver, the incoming signals are filtered, amplified, and then applied to the demodulator and decoder circuits, which extracts the original source information from the modulated carrier. The clock and carrier recovery circuits recover the analog carrier and digital timing (clock) signals from the incoming modulated wave as they are necessary to perform the demodulation process.

**INFORMATION CAPACITY, BITS, BIT RATE, BAUD AND MINIMUM BANDWIDTH**

**Information Capacity, Bits, and Bit Rate**

The information capacity of a data communications system can be determined by Information theory. **"Information capacity is a measure of how much information can be propagated through a communications system and is a function of bandwidth and transmission time**."

The information is represented by the binary digit, or bit. Therefore, it is convenient to express the information capacity of a system as a bit rate. "**<u>Bit rate is simply the number of bits transmitted during one second and is expressed in bits per second (bps).</u>**"

The relationship between bandwidth, transmission time, and information capacity is given by Hartley's law which is written as

$$\mathbf{I \propto B \times t}$$

Where

I = information capacity (bits per second)
B = bandwidth (hertz)
t = transmission time (seconds)

From the above equation, it can be seen that information capacity is a linear function of bandwidth and transmission time and is directly proportional to both.

The relation between the information capacity of a communication channel to bandwidth and signal-to-noise ratio is expressed mathematically as

$$I = B \log_2\left(1 + \frac{S}{N}\right)$$

or

$$I = 3.32B \log_{10}\left(1 + \frac{S}{N}\right)$$

where $I$ = information capacity (bps)
$B$ = bandwidth (hertz)
$\frac{S}{N}$ = signal-to-noise power ratio (unitless)

**This is known as the Shannon limit for information capacity.**

## <u>Baud and Minimum Bandwidth:</u>

**<u>Baud refers to the rate of change of a signal on the transmission medium after encoding and modulation have occurred.</u>** Hence, baud is a unit of transmission rate, modulation rate, or symbol rate.

Mathematically, baud is the reciprocal of the time of one output signaling element, and a signaling element may represent several information bits. Baud is expressed as

$$\text{baud} = \frac{1}{t_s}$$

where baud = symbol rate (baud per second)
$t_s$ = time of one signaling element (seconds)

The minimum theoretical bandwidth necessary to propagate a signal is called **the minimum Nyquist bandwidth or the minimum Nyquist frequency**.

Thus, $f_b = 2B$, where

$f_b$ = the bit rate in bps and

$B$ = the ideal Nyquist bandwidth.

For a given bandwidth (B), the highest theoretical bit rate is 2B. However, if more than two levels are used for signaling (higher-than-binary encoding), more than one bit may be transmitted at a time, and it is possible to propagate a bit rate that exceeds 2B. Using multilevel signaling, the Nyquist formulation for channel capacity is

$$f_b = 2B \log_2 M \quad (8)$$

where $f_b$ = channel capacity (bps)
$B$ = minimum Nyquist bandwidth (hertz)
$M$ = number of discrete signal or voltage levels

Equation 8 can be rearranged to solve for the minimum bandwidth necessary to pass $M$-ary digitally modulated carriers

$$B = \left(\frac{f_b}{\log_2 M}\right) \quad (9)$$

If $N$ is substituted for $\log_2 M$, Equation 9 reduces to

$$B = \frac{f_b}{N} \quad (10)$$

where $N$ is the number of bits encoded into each signaling element.

If information bits are encoded (grouped) and then converted to signals with more than two levels, transmission rates in excess of 2B are possible. In addition, since baud is the encoded rate of change, it also equals the bit rate divided by the number of bits encoded into one signaling element. Thus,

$$\text{baud} = \frac{f_b}{N} \quad (11)$$

By comparing Equation 10 with Equation 11, it can be seen that with digital modulation, the baud and the ideal minimum Nyquist bandwidth have the same value and are equal to the bit rate divided by the number of bits encoded

**AMPLITUDE-SHIFT KEYING:**

**Amplitude-shift keying (ASK) is a digital modulation technique in which a binary information signal directly modulates the amplitude of an analog carrier.**

Mathematically it is represented as

$$v_{(ask)}(t) = [1 + v_m(t)]\left[\frac{A}{2}\cos(\omega_c t)\right] \qquad (12)$$

where $v_{ask}(t)$ = amplitude-shift keying wave
$v_m(t)$ = digital information (modulating) signal (volts)
$A/2$ = unmodulated carrier amplitude (volts)
$\omega_c$ = analog carrier radian frequency (radians per second, $2\pi f_c t$)

In Equation 12, the modulating signal $v_m(t)$ is a normalized binary waveform, where +1 V = logic 1 and -1 V = logic 0. Therefore, for a logic 1 input, $v_m(t)$ = + 1 V, Equation 12 reduces to

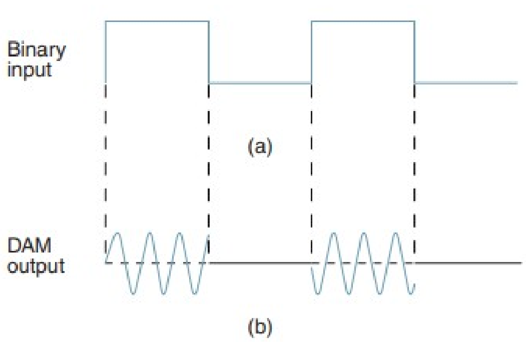
$$v_{(ask)}(t) = [1 + 1]\left[\frac{A}{2}\cos(\omega_c t)\right]$$
$$= A\cos(\omega_c t)$$

and for a logic 0 input, $v_m(t) = -1$ V, Equation 12 reduces to

$$v_{(ask)}(t) = [1 - 1]\left[\frac{A}{2}\cos(\omega_c t)\right]$$
$$= 0$$

Thus, the modulated wave $v_{ask}(t)$, is either A cos ($\omega_c$t) or 0. Hence, the carrier is either "on" or "off". Hence it is also referred to as on-off keying (OOK).

The input and output waveforms from an ASK modulator as shown below.




From the figure, it can be seen that for every change in the input binary data stream, there is one change in the ASK waveform, and the time of one bit ($t_b$) equals the time of one analog signaling element ($t_s$).

The bit time is the reciprocal of the bit rate and the time of one signaling element is the reciprocal of the baud. Therefore, the rate of change of the ASK waveform (baud) is the same as the rate of change of the binary input (bps); thus, the bit rate equals the baud.

$$B = \frac{f_b}{1} = f_b \qquad \text{baud} = \frac{f_b}{1} = f_b$$

### Example 1

Determine the baud and minimum bandwidth necessary to pass a 10 kbps binary signal using amplitude shift keying.

**Solution** For ASK, $N = 1$, and the baud and minimum bandwidth are determined from Equations 11 and 10, respectively:

$$B = \frac{10{,}000}{1} = 10{,}000$$

$$\text{baud} = \frac{10{,}000}{1} = 10{,}000$$

## FREQUENCY-SHIFT KEYING

**Frequency-shift keying (FSK) is one in which the modulating signal is a binary signal that varies between two discrete voltage levels.** Hence, FSK is sometimes called binary FSK (BFSK). The general expression for FSK is

$$v_{fsk}(t) = V_c \cos\{2\pi[f_c + v_m(t)\,\Delta f]t\} \qquad (13)$$

where $v_{fsk}(t)$ = binary FSK waveform
$V_c$ = peak analog carrier amplitude (volts)
$f_c$ = analog carrier center frequency (hertz)
$\Delta f$ = peak change (shift) in the analog carrier frequency (hertz)
$v_m(t)$ = binary input (modulating) signal (volts)

From Equation 13, it can be seen that the peak shift in the carrier frequency (Δf) is proportional to the amplitude of the binary input signal $v_m(t)$, and the direction of the shift is determined by the polarity.

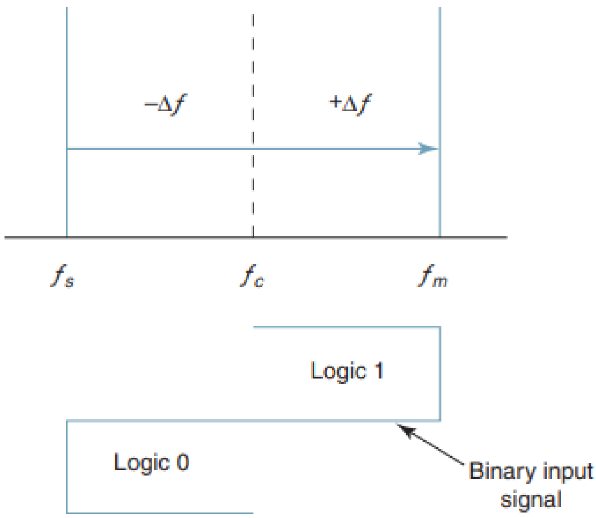
The modulating signal is a normalized binary waveform where a logic 1= +1 V and a logic 0 = - 1 V. Thus, for a logic 1 input, $v_m(t) = +1$, Equation 13 can be rewritten as

$$v_{fsk}(t) = V_c \cos[2\pi(f_c + \Delta f)t]$$

For a logic 0 input, $v_m(t) = -1$, Equation 13 becomes

$$v_{fsk}(t) = V_c \cos[2\pi(f_c - \Delta f)t]$$

With binary FSK, the carrier center frequency (fc) is shifted (deviated) up and down in the frequency domain by the binary input signal as shown in Figure




As the binary input signal changes from a logic 0 to a logic 1 and vice versa, the output frequency shifts between two frequencies: a Mark, or logic 1 frequency (fm), and a Space, or logic 0 frequency (fs). The mark and space frequencies are separated from the carrier frequency by the peak frequency deviation (Δf) and from each other by **2 Δf**.

**Frequency deviation:**

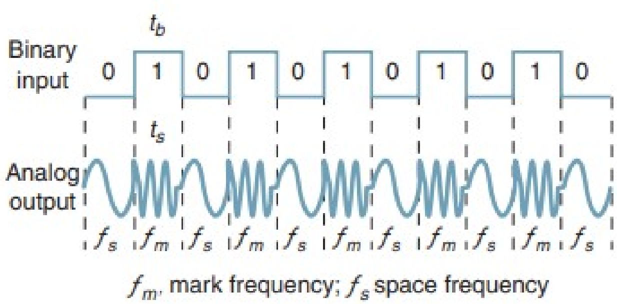
**Frequency deviation is defined as the difference between either the mark or space frequency and the center frequency.** It is expressed mathematically as

$$\Delta f = \frac{|f_m - f_s|}{2} \qquad (14)$$

where $\Delta f$ = frequency deviation (hertz)

$|f_m - f_s|$ = absolute difference between the mark and space frequencies (hertz)

The input and output waveforms of an FSK modulator in time domain is as shown below.




(a)

| binary input | frequency output |
|---|---|
| 0 | space ($f_s$) |
| 1 | mark ($f_m$) |

(b)

FIGURE 4 FSK in the time domain: (a) waveform; (b) truth table

When the binary input (fb) changes from a logic 1 to a logic 0 and vice versa, the FSK output frequency shifts from a mark (fm) to a space (fs) frequency and vice versa. In Figure, the mark frequency is the higher frequency (fc + Δf), and the space frequency is the lower frequency (fc - Δf). The truth table for a binary FSK modulator is as shown above.

## FSK Bit Rate, Baud, and Bandwidth

From the above Figure, it is observed that the time of one bit ($t_b$) is the same as the time the FSK output is a mark or space frequency ($t_s$). Thus, the bit time equals the time of an FSK signaling element, and the bit rate equals the baud.

The baud for binary FSK can also be determined by substituting N = 1 in Equation 11:

$$\text{baud} = \frac{f_b}{1} = f_b$$

FSK is the exception to the rule for digital modulation, as the minimum bandwidth is not determined from Equation 10. The minimum bandwidth for FSK is given as

$$B = |(f_s - f_b) - (f_m - f_b)|$$
$$= |f_s - f_m| + 2f_b$$

and since $|f_s - f_m|$ equals $2\Delta f$, the minimum bandwidth can be approximated as

$$B = 2(\Delta f + f_b) \quad (15)$$

where $B$ = minimum Nyquist bandwidth (hertz)
$\Delta f$ = frequency deviation ($|f_m - f_s|$) (hertz)
$f_b$ = input bit rate (bps)

**Example 2**

Determine (a) the peak frequency deviation, (b) minimum bandwidth, and (c) baud for a binary FSK signal with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

**Solution** a. The peak frequency deviation is determined from Equation 14:

$$\Delta f = \frac{|49\text{kHz} - 51\text{kHz}|}{2}$$
$$= 1\text{ kHz}$$

b. The minimum bandwidth is determined from Equation 15:

$$B = 2(1000 + 2000)$$
$$= 6\text{ kHz}$$

c. For FSK, $N = 1$, and the baud is determined from Equation 11 as

$$\text{baud} = \frac{2000}{1} = 2000$$

Bessel functions can also be used to determine the approximate bandwidth for an FSK wave. The highest fundamental frequency in a nonreturn-to-zero (NRZ) binary signal occurs when alternating 1s and 0s are occurring (i.e., a square wave). Since it takes a high and a low to produce a cycle, the highest fundamental frequency present in a square wave equals the repetition rate of the square wave, which with a binary signal is equal to half the bit rate. Therefore,

$$f_a = \frac{f_b}{2} \quad (16)$$

where $f_a$ = highest fundamental frequency of the binary input signal (hertz)
$f_b$ = input bit rate (bps)

The formula used for modulation index in FM is also valid for FSK; thus,

$$h = \frac{\Delta f}{f_a} \quad \text{(unitless)} \quad (17)$$

where $h$ = FM modulation index called the h-factor in FSK
$f_a$ = fundamental frequency of the binary modulating signal (hertz)
$\Delta f$ = peak frequency deviation (hertz)

The worst-case modulation index which is called the  deviation ratio occurs when both the frequency deviation and the modulating-signal frequency are at their maximum values. This results in the widest bandwidth.. Thus,

$$h = \frac{\frac{|f_m - f_s|}{2}}{\frac{f_b}{2}} \quad \text{(unitless)}$$

r

$$h = \frac{|f_m - f_s|}{f_b} \quad (18)$$

where $h$ = h-factor (unitless)
$f_m$ = mark frequency (hertz)
$f_s$ = space frequency (hertz)
$f_b$ = bit rate (bits per second)

**Example 3**

Using a Bessel table, determine the minimum bandwidth for the same FSK signal described in Example 1 with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

**Solution** The modulation index is found by substituting into Equation 17:

or

$$h = \frac{|49\text{ kHz} - 51\text{ kHz}|}{2\text{ kbps}} = \frac{2\text{ kHz}}{2\text{ kbps}} = 1$$

From a Bessel table, three sets of significant sidebands are produced for a modulation index of one. Therefore, the bandwidth can be determined as follows:

$$B = 2(3 \times 1000) = 6000\text{ Hz}$$

## FSK Transmitter

The binary FSK modulator is as shown below.

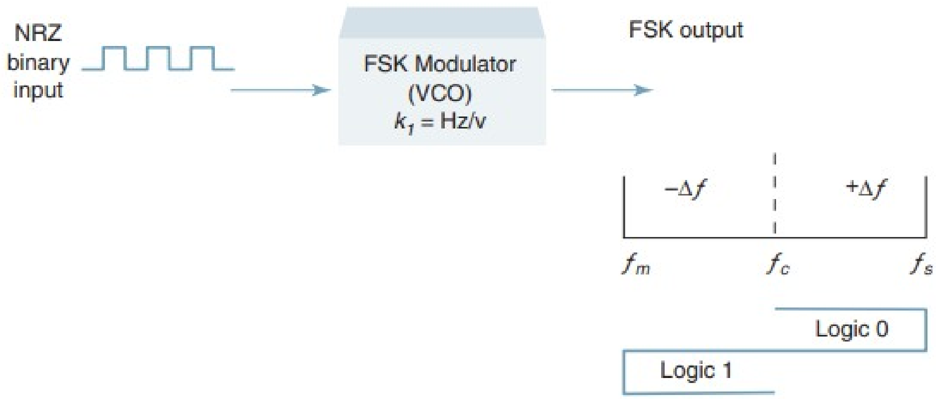



FIGURE 6 FSK modulator

The key circuit is a voltage-controlled oscillator (VCO). The center frequency (fc) is chosen such that it falls halfway between the mark and space frequencies. Logic 1 input shifts the VCO output to the mark frequency, and a logic 0 input shifts the VCO output to the space frequency. Consequently, as the binary input signal changes back and forth between logic 1 and logic 0 conditions, the VCO output deviates back and forth between the mark and space frequencies.

In a binary FSK modulator, Δf is the peak frequency deviation of the carrier and is equal to the difference between the carrier rest frequency and either the mark or the space frequency AVCOFSK modulator is operated in the sweep mode where the peak frequency deviation is simply the product of the binary input voltage and the deviation sensitivity of the VCO. With the sweep mode of modulation, the frequency deviation is expressed mathematically as

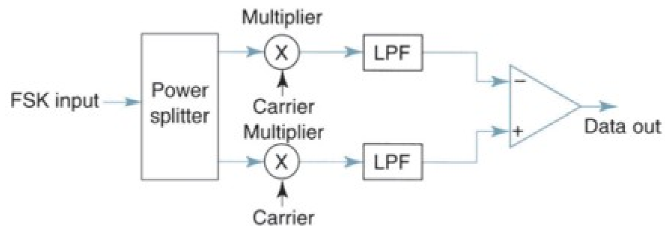
$$\Delta f = v_m(t)k_l \qquad (19)$$

where $\Delta f$ = peak frequency deviation (hertz)
$v_m(t)$ = peak binary modulating-signal voltage (volts)
$k_l$ = deviation sensitivity (hertz per volt).

With binary FSK, the amplitude of the input signal can only be one of two values, one for a logic 1 condition and one for a logic 0 condition. Therefore, the peak frequency deviation is constant and always at its maximum value.

## FSK Receiver

The block diagram for a coherent FSK receiver is as shown below.




The incoming FSK signal is multiplied by a recovered carrier signal that has the exact same frequency and phase as the transmitter reference. However, the two transmitted frequencies (the mark and space frequencies) are not generally continuous; it is not practical to reproduce a local reference that is coherent with both of them. Consequently, coherent FSK detection is seldom used.

## PHASE-SHIFT KEYING

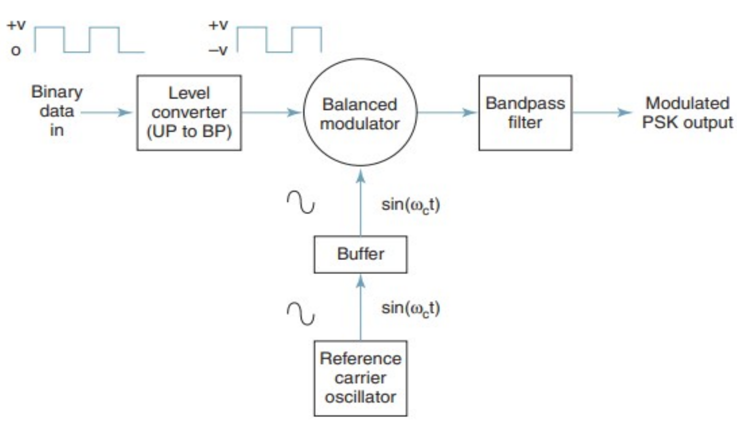
**Phase-shift keying (PSK) is a digital modulation process which conveys data by changing (modulating) the phase of a constant frequency carrier wave.** The input binary information is encoded into groups of bits before modulating the carrier. The number of bits in a group ranges from 1 to 12 or more. The number of output phases is defined by M where M is number of conditions, levels, or combinations possible with N bits and determined by the number of bits in the group (n).

### Binary Phase-Shift Keying

The simplest form of PSK is binary phase-shift keying (BPSK), where N= 1 and M = 2. Therefore, with BPSK, two phases ($2^1 = 2$) are possible for the carrier. One phase represents a logic 1, and the other phase represents a logic 0. As the input digital signal changes state (i.e., from a 1 to a 0 or from a 0 to a 1), the phase of the output carrier shifts between two angles that are separated by 180°.

### BPSK transmitter.

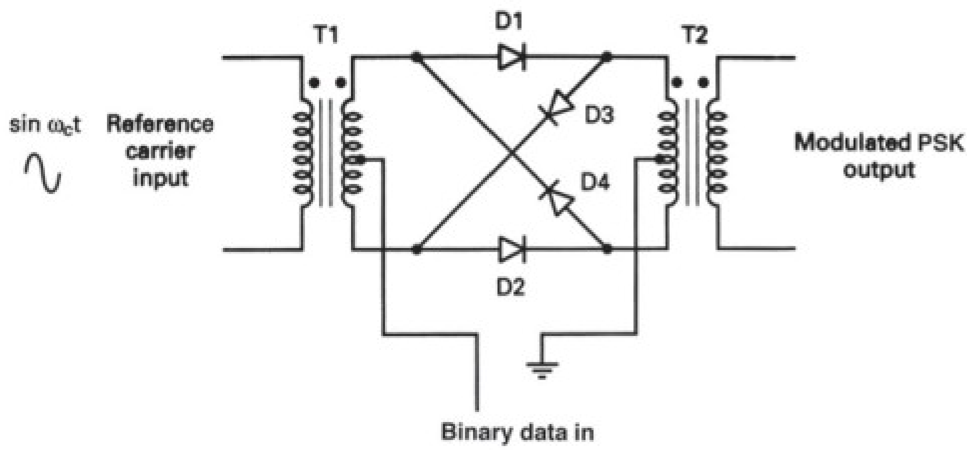
The block diagram of a BPSK transmitter is as shown below




The balanced modulator acts as a phase reversing switch. Depending on the logic condition of the digital input, the carrier is transferred to the output either in phase or 180° out of phase with the reference carrier oscillator

**Working of Balanced Ring Modulator**

The schematic diagram of a balanced ring modulator is as shown below




The balanced modulator has two inputs:

- A carrier that is in phase with the reference oscillator and
- The binary digital data.

For the balanced modulator to operate, the digital input voltage must be much greater than the peak carrier voltage. This ensures that the digital input controls the on/off state of diodes D1 to D4.

**Condition 1 - the binary input is logic 1**

If the binary input is a logic 1 (positive voltage), diodes D1 and D2 are forward biased and on, while diodes D3 and D4 are reverse biased and off. The carrier voltage is developed across transformer T2 in phase with the carrier voltage across T1. Consequently, the output signal is in phase with the reference oscillator.

**Condition 2 - the binary input is logic 0**

If the binary input is a logic 0 (negative voltage), diodes D1 and D2 are reverse biased and off, while diodes D3 and D4 are forward biased and on . As a result, the carrier voltage is developed across transformer T2 180° out of phase with the carrier voltage across T1. Consequently, the output signal is 180° out of phase with the reference oscillator.

The truth table, phasor diagram, and constellation diagram for a BPSK modulator is as shown below.

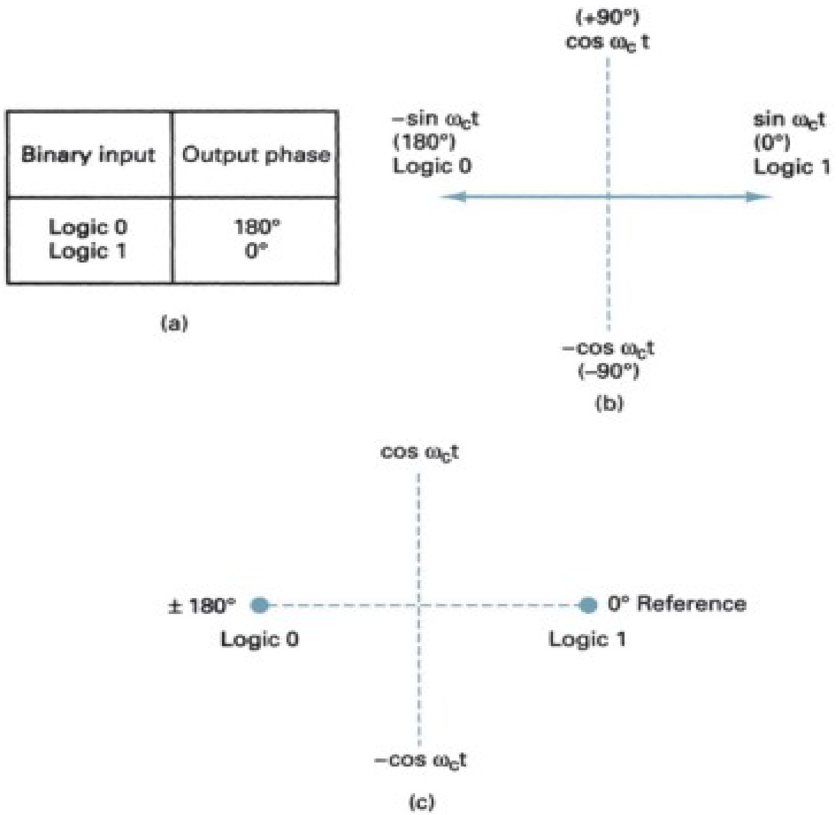



FIGURE 14 BPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

**<u>Bandwidth considerations of BPSK.</u>**

A balanced modulator is a *product modulator*, that is, the output signal is the product of the two input signals. In a BPSK modulator, the carrier input signal is multiplied by the binary data. If +1 V is assigned to a logic 1 and -1 V is assigned to a logic 0, the input carrier (sin $\omega_c$t) is multiplied by either a +1 or -1. Consequently, the output signal is either +1 sin $\omega_c$t which represents a signal that is in phase with the reference oscillator or -1 sin $\omega_c$t which represents a signal that is 180° out of phase with the reference oscillator. Consequently, for BPSK, the output rate of change (baud) is equal to the input rate of change (bps), and the widest output bandwidth occurs when the input binary data are an alternating 1/0 sequence. The fundamental frequency ( fa) of an alternative 1/0 bit sequence is equal to one-half of the bit rate ( fb/2). Mathematically, the output of a BPSK modulator is proportional to

$$\text{BPSK output} = [\sin(2\pi f_a t)] \times [\sin(2\pi f_c t)] \qquad (20)$$

where $f_a$ = maximum fundamental frequency of binary input (hertz)
$f_c$ = reference carrier frequency (hertz)

Solving for the trig identity for the product of two sine functions,

$$\frac{1}{2}\cos[2\pi(f_c - f_a)t] - \frac{1}{2}\cos[2\pi(f_c + f_a)t]$$

Thus, the minimum double-sided Nyquist bandwidth ($B$) is

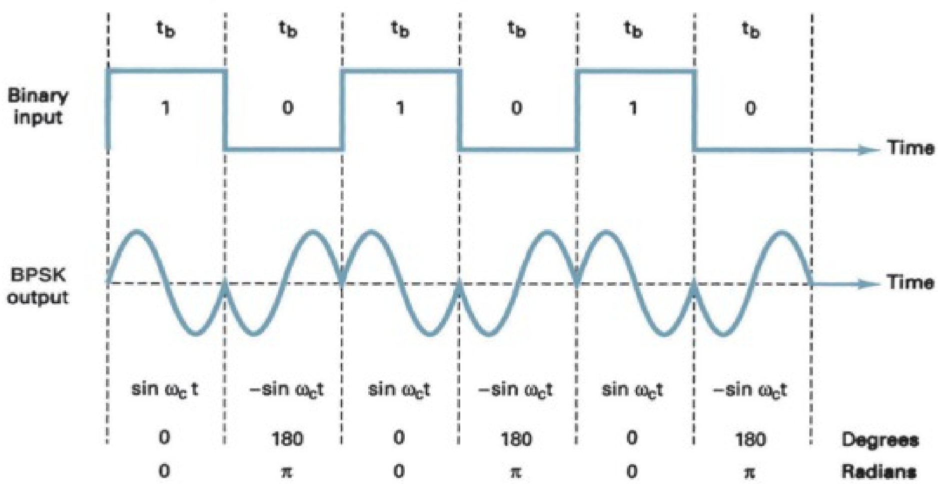
$$\begin{array}{r} f_c + f_a \\ -(f_c + f_a) \\ \hline \end{array} \quad \text{or} \quad \begin{array}{r} f_c + f_a \\ -f_c + f_a \\ \hline 2f_a \end{array}$$

and because $f_a = f_b/2$, where $f_b$ = input bit rate,

$$B = \frac{2f_b}{2} = f_b$$

where $B$ is the minimum double-sided Nyquist bandwidth.

The following figure shows the relationship of output phase-versus-time for a BPSK waveform.




As the figure shows, a logic 1 input produces an analog output signal with a 0° phase angle, and a logic 0 input produces an analog output signal with a 180° phase angle. As the binary input shifts between a logic 1 and a logic 0 condition and vice versa, the phase of the BPSK waveform shifts between 0° and 180°, respectively.

**Example 4**

**For a BPSK modulator with a carrier frequency of 70 MHz and an input bit rate of 10 Mbps, determine the maximum and minimum upper and lower side frequencies, draw the output spectrum, determine the minimum Nyquist bandwidth, and calculate the baud.**

**Solution** Substituting into Equation 20 yields

$$\text{output} = (\sin \omega_a t)(\sin \omega_c t)$$
$$= [\sin 2\pi(5\text{ MHz})t][\sin 2\pi(70\text{ MHz})t]$$

$$= \underbrace{\frac{1}{2}\cos 2\pi(70\text{ MHz} - 5\text{ MHz})t}_{\text{lower side frequency}} - \underbrace{\frac{1}{2}\cos 2\pi(70\text{ MHz} + 5\text{ MHz})t}_{\text{upper side frequency}}$$

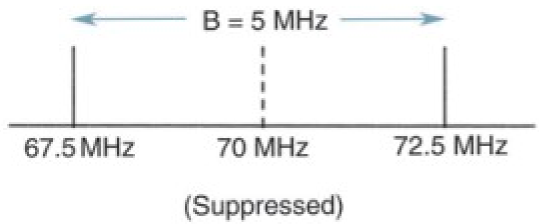
Minimum lower side frequency (LSF):

$$\text{LSF} = 70\text{ MHz} - 5\text{ MHz} = 65\text{ MHz}$$

Maximum upper side frequency (USF):

$$\text{USF} = 70\text{ MHz} + 5\text{ MHz} = 75\text{ MHz}$$

Therefore, the output spectrum for the worst-case binary input conditions is as follows:
The minimum Nyquist bandwidth ($B$) is

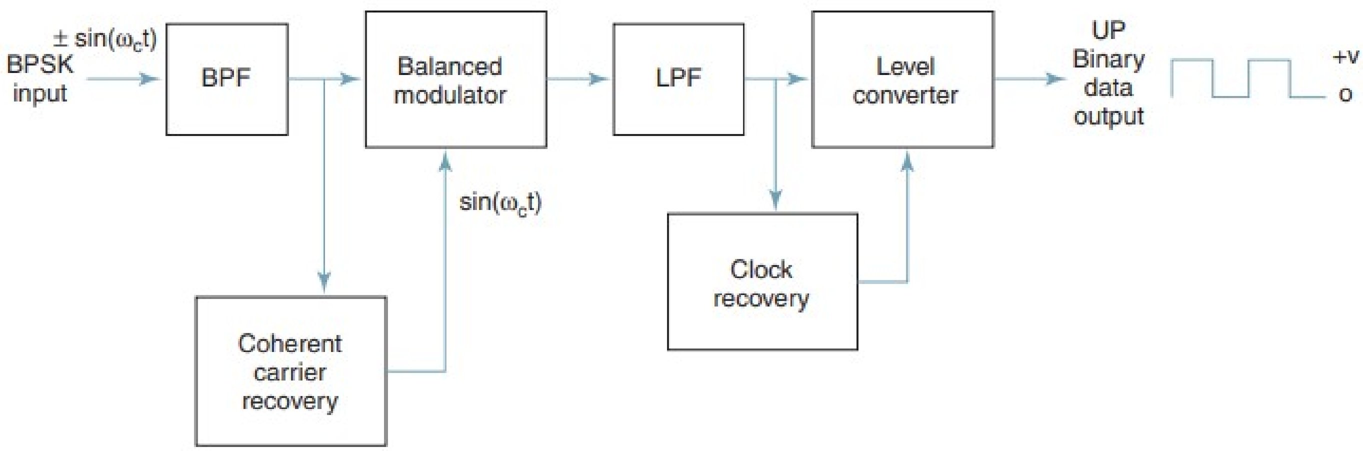



$$B = 75\text{ MHz} - 65\text{ MHz} = 10\text{ MHz}$$

and the baud = $f_b$ or 10 megabaud.

**BPSK receiver**

The block diagram of a BPSK receiver is as shown below




The input signal may be **+ sin $\omega_c$t** or **- sin $\omega_c$t**. The coherent carrier recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier.

The balanced modulator is a product detector; the output is the product of the two inputs (the BPSK signal and the recovered carrier).

The low-pass filter (LPF) separates the recovered binary data from the complex demodulated signal. Mathematically, the demodulation process is as follows.

For a BPSK input signal of **+ sin $\omega_c$t** (logic 1), the output of the balanced modulator is

$$\text{output} = (\sin \omega_c t)(\sin \omega_c t) = \sin^2 \omega_c t$$

or $$\sin^2 \omega_c t = \frac{1}{2}(1 - \cos 2\omega_c t) = \frac{1}{2} - \underset{\text{(filtered out)}}{\frac{1}{2}\cos 2\omega_c t}$$

leaving $$\text{output} = +\frac{1}{2}\text{V} = \text{logic 1}$$

It can be seen that the output of the balanced modulator contains a positive voltage (+[1/2]V) and a cosine wave at twice the carrier frequency (2 $\omega_c$). The LPF has a cutoff frequency much lower than 2 $\omega_c$ and thus, blocks the second harmonic of the carrier and passes only the positive constant component. A positive voltage represents a demodulated logic 1.

For a BPSK input signal of $-\sin \omega_c t$ (logic 0), the output of the balanced modulator is

$$\text{output} = (-\sin \omega_c t)(\sin \omega_c t) = -\sin^2 \omega_c t$$

or $$-\sin^2 \omega_c t = -\frac{1}{2}(1 - \cos 2\omega_c t) = -\frac{1}{2} + \underset{\text{(filtered out)}}{\frac{1}{2}\cos 2\omega_c t}$$

leaving $$\text{output} = -\frac{1}{2}\text{V} = \text{logic 0}$$

The output of the balanced modulator contains a negative voltage (-[1/2]V) and a cosine wave at twice the carrier frequency (2 $\omega_c$). Again, the LPF blocks the second harmonic of the carrier and passes only the negative constant component. A negative voltage represents a demodulated logic 0.

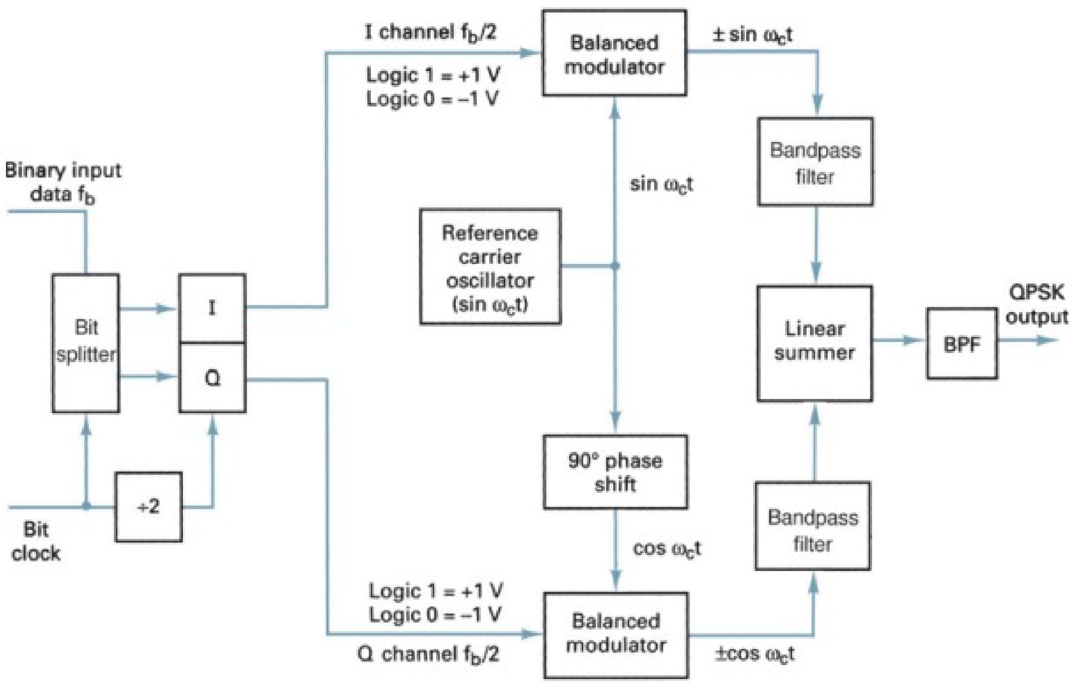
**Quaternary (Quadrature) Phase-Shift Keying**

**Quadrature Phase Shift Keying (QPSK) is a form of Phase Shift Keying in which two bits are modulated at once, selecting one of four possible carrier phase**. In QPSK, four output phases (+45°, +135°, - 45°, and - 135°) are possible for a single carrier frequency. Because there are four output phases, the modulator requires four different input conditions. With two bits, there are four possible conditions: 00, 01, 10, and 11. Therefore, with QPSK, the binary input data are combined into groups of two bits, called **dibits.** In the modulator, each dibit code generates one of the four possible output phases (+45°, +135°, -

45°, and - 135°). Therefore, for each two-bit dibit clocked into the modulator, a single output change occurs, and the rate of change at the output (baud) is equal to one-half the input bit rate

**QPSK transmitter.**

A block diagram of a QPSK modulator is shown in Figure




Two bits (a dibit) are clocked into the bit splitter. After both bits have been serially inputted, they are simultaneously parallel outputted. One bit is directed to the I channel and the other to the Q channel. The I bit modulates a carrier that is in phase with the reference oscillator (hence the name "I" for "in phase" channel), and the Q bit modulates a carrier that is 90° out of phase or in Quadrature with the reference carrier (hence the name "Q" for "quadrature" channel).

A QPSK modulator is two BPSK modulators combined in parallel. Two phases are possible at the output of the I balanced modulator (+sin $\omega_c$t and - sin $\omega_c$t) for a logic 1= + 1 V and a logic 0 = -1 V. Similarly, two phases are possible at the output of the Q balanced modulator (+cos $\omega_c$t and - cos $\omega_c$t). When the linear summer combines the two Quadrature (90° out of phase) signals, there are four possible resultant phasors given by these expressions:

- $+\sin \omega_c t \; +\cos \omega_c t$,
- $+\sin \omega_c t \; -\cos \omega_c t$,
- $-\sin \omega_c t \; +\cos \omega_c t$, and
- $\sin \omega_c t \; -\cos \omega_c t$.

### Example 5

For the QPSK modulator shown in Figure 17, construct the truth table, phasor diagram, and constellation diagram.

**Solution** For a binary data input of Q = 0 and I = 0, the two inputs to the I balanced modulator are $-1$ and $\sin \omega_c t$, and the two inputs to the Q balanced modulator are $-1$ and $\cos \omega_c t$. Consequently, the outputs are

$$\text{I balanced modulator} = (-1)(\sin \omega_c t) = -1 \sin \omega_c t$$
$$\text{Q balanced modulator} = (-1)(\cos \omega_c t) = -1 \cos \omega_c t$$

and the output of the linear summer is

$$-1 \cos \omega_c t - 1 \sin \omega_c t = 1.414 \sin(\omega_c t - 135°)$$

For the remaining dibit codes (01, 10, and 11), the procedure is the same. The results are shown in Figure 18a.

| Binary input Q | Binary input I | QPSK output phase |
|---|---|---|
| 0 | 0 | −135° |
| 0 | 1 | −45° |
| 1 | 0 | +135° |
| 1 | 1 | +45° |

(a)

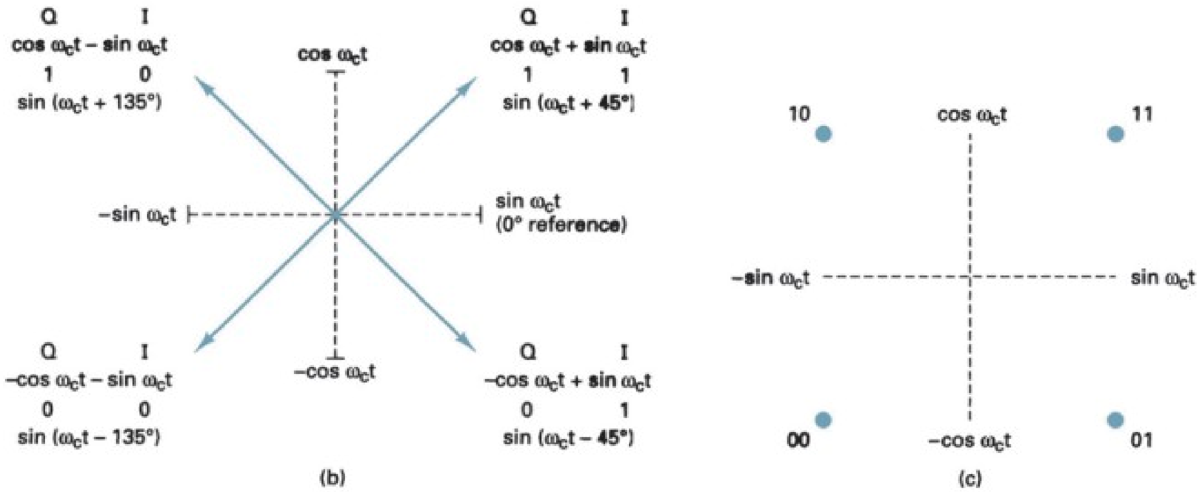



FIGURE 18 QPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

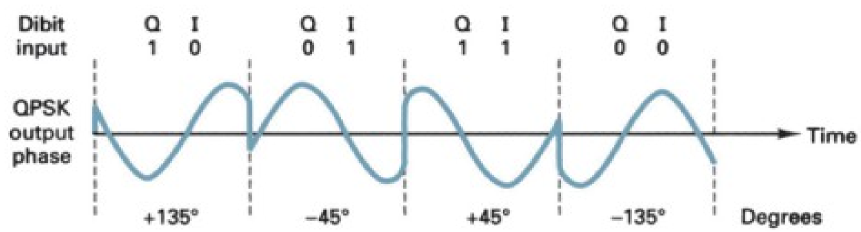
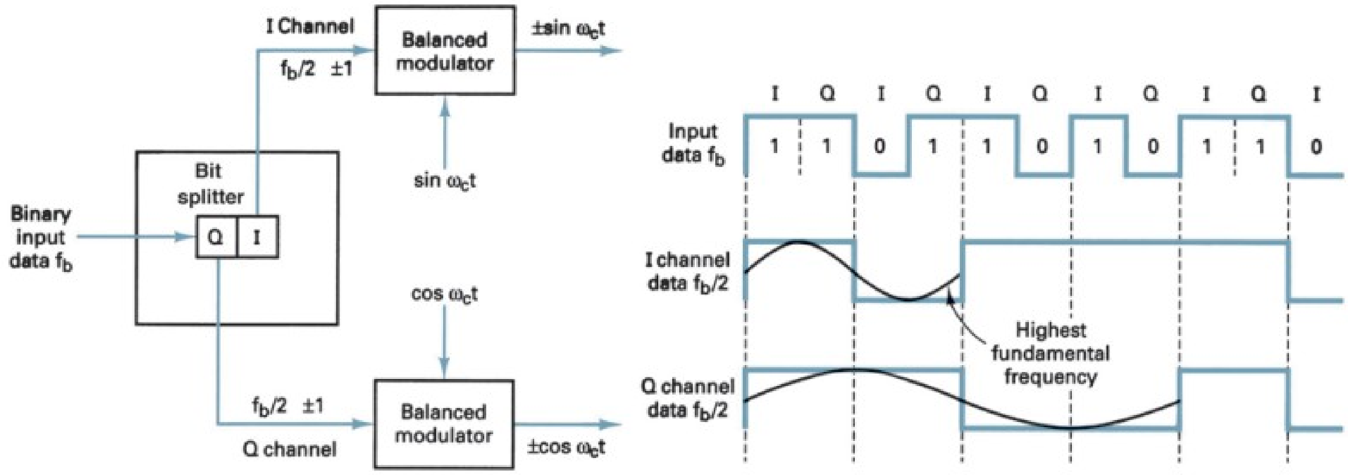



FIGURE 19 Output phase-versus-time relationship for a QPSK modulator

**Bandwidth considerations of QPSK.**

- With QPSK, because the input data are divided into two channels, the bit rate in either the I or the Q channel is equal to one-half of the input data rate (fb/2).
- Consequently, the highest fundamental frequency present at the data input to the I or the Q balanced modulator is = fb/4.
- As a result, the output of the I and Q balanced modulators requires a minimum double-sided Nyquist bandwidth equal to one-half of the incoming bit rate ($f_N$ = 2 x fb/4 = fb/2).
- . This relationship is shown in the following Figure




- In the above Figure, it can be seen that the worse-case input condition to the I or Q balanced modulator is an alternative 1/0 pattern.
- 1/0 pattern, which occurs when the binary input data have a 1100 repetitive pattern. One cycle of the fastest binary transition (a 1/0 sequence in the I or Q channel takes the same time as four input data bits.
- Consequently, the highest fundamental frequency at the input and fastest rate of change at the output of the balance modulators is equal to one-fourth of the binary input bit rate.

The output of the balanced modulators can be expressed mathematically as

$$\text{output} = (\sin \omega_a t)(\sin \omega_c t) \tag{22}$$

where

$$\underbrace{\omega_a t = 2\pi \frac{f_b}{4} t}_{\text{modulating signal}} \quad \text{and} \quad \underbrace{\omega_c t = 2\pi f_c}_{\text{carrier}}$$

Thus,

$$\text{output} = \left(\sin 2\pi\frac{f_b}{4}t\right)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi\left(f_c - \frac{f_b}{4}\right)t - \frac{1}{2}\cos 2\pi\left(f_c + \frac{f_b}{4}\right)t$$

The output frequency spectrum extends from $f_c + f_b/4$ to $f_c - f_b/4$, and the minimum bandwidth ($f_N$) is

$$\left(f_c + \frac{f_b}{4}\right) - \left(f_c - \frac{f_b}{4}\right) = \frac{2f_b}{4} = \frac{f_b}{2}$$

### Example 6

For a QPSK modulator with an input data rate ($f_b$) equal to 10 Mbps and a carrier frequency of 70 MHz, determine the minimum double-sided Nyquist bandwidth ($f_N$) and the baud. Also, compare the results with those achieved with the BPSK modulator in Example 4. Use the QPSK block diagram shown in Figure 17 as the modulator model.

**Solution** The bit rate in both the I and Q channels is equal to one-half of the transmission bit rate, or

$$f_{bQ} = f_{bI} = \frac{f_b}{2} = \frac{10 \text{ Mbps}}{2} = 5 \text{ Mbps}$$

The highest fundamental frequency presented to either balanced modulator is

$$f_a = \frac{f_{bQ}}{2} \text{ or } \frac{f_{bI}}{2} = \frac{5 \text{ Mbps}}{2} = 2.5 \text{ MHz}$$

The output wave from each balanced modulator is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi(f_c - f_a)t - \frac{1}{2}\cos 2\pi(f_c + f_a)t$$

$$\frac{1}{2}\cos 2\pi[(70 - 2.5) \text{ MHz}]t - \frac{1}{2}\cos 2\pi[(70 + 2.5) \text{ MHz}]t$$

$$\frac{1}{2}\cos 2\pi(67.5 \text{ MHz})t - \frac{1}{2}\cos 2\pi(72.5 \text{ MHz})t$$

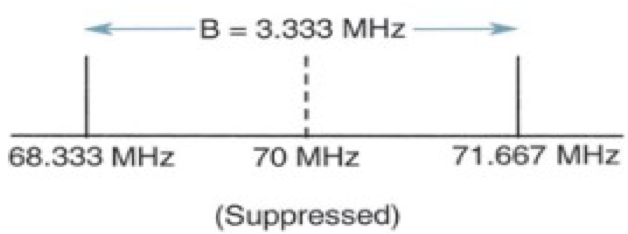
The minimum Nyquist bandwidth is

$$B = (72.5 - 67.5) \text{ MHz} = 5 \text{ MHz}$$

The symbol rate equals the bandwidth; thus,

$$\text{symbol rate} = 5 \text{ megabaud}$$

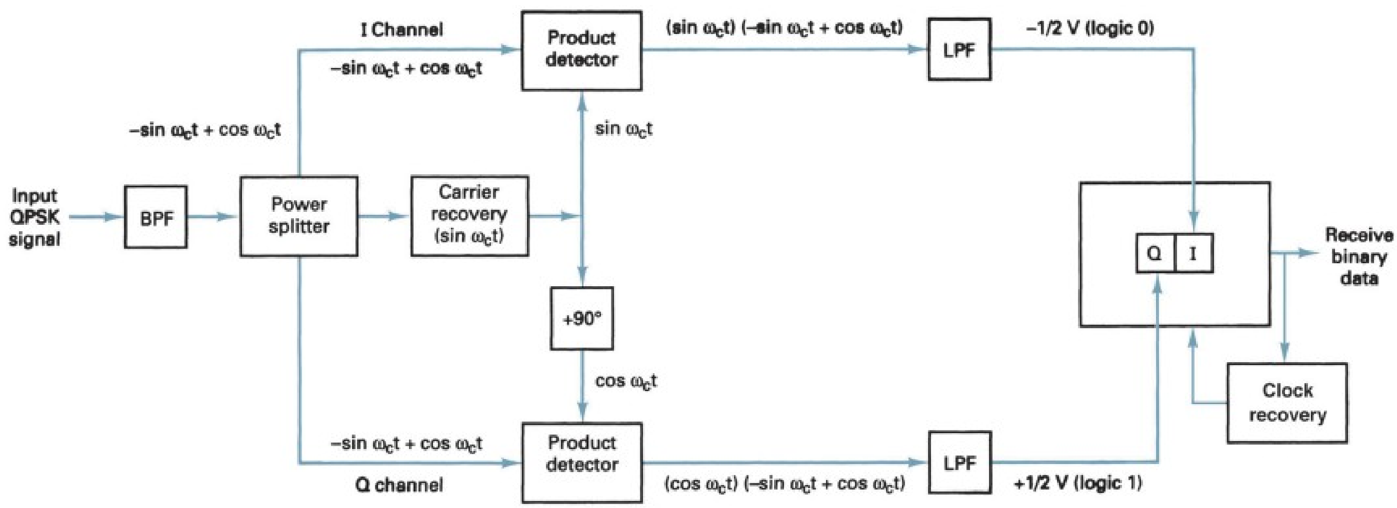
The output spectrum is as follows:




$$B = 5 \text{ MHz}$$

## QPSK receiver

The block diagram of a QPSK receiver is shown in the following Figure




- The power splitter directs the input QPSK signal to the I and Q product detectors and the carrier recovery circuit.
- The carrier recovery circuit reproduces the original transmit carrier oscillator signal.
- The recovered carrier must be frequency and phase coherent with the transmit reference carrier.
- The QPSK signal is demodulated in the I and Q product detectors, which generate the original I and Q data bits.
- The outputs of the product detectors are fed to the bit combining circuit, where they are converted from parallel I and Q data channels to a single binary output data stream.
- The incoming QPSK signal may be any one of the four possible output phases

To illustrate the demodulation process, let the incoming QPSK signal be sin $\omega_c t$ cos $\omega_c t$. Mathematically, the demodulation process is as follows.

The receive QPSK signal (sin $\omega_c t$ cos $\omega_c t$) is one of the inputs to the I product detector. The other input is the recovered carrier (sin $\omega_c t$). The output of the I product detector is

$$\mathrm{I} = \underbrace{(-\sin \omega_c t + \cos \omega_c t)}_{\text{QPSK input signal}} \underbrace{(\sin \omega_c t)}_{\text{carrier}} \quad (23)$$

$$= (-\sin \omega_c t)(\sin \omega_c t) + (\cos \omega_c t)(\sin \omega_c t)$$

$$= -\sin^2 \omega_c t + (\cos \omega_c t)(\sin \omega_c t)$$

$$= -\frac{1}{2}(1 - \cos 2\omega_c t) + \frac{1}{2}\sin(\omega_c + \omega_c)t + \frac{1}{2}\sin(\omega_c - \omega_c)t$$

$$\mathrm{I} = -\frac{1}{2} + \frac{1}{2}\underbrace{\cos 2\omega_c t}_{\text{(filtered out)}} + \frac{1}{2}\sin 2\omega_c t + \frac{1}{2}\underbrace{\sin 0}_{\text{(equals 0)}}$$

$$= -\frac{1}{2}\mathrm{V} \text{ (logic 0)}$$

Again, the receive QPSK signal ($\sin \omega_c t \cos \omega_c t$) is one of the inputs to the Q product detector. The other input is the recovered carrier shifted 90° in phase ($\cos \omega_c t$). The output of the Q product detector is

$$\mathrm{Q} = \underbrace{(-\sin \omega_c t + \cos \omega_c t)}_{\text{QPSK input signal}} \underbrace{(\cos \omega_c t)}_{\text{carrier}} \quad (24)$$

$$= \cos^2 \omega_c t - (\sin \omega_c t)(\cos \omega_c t)$$

$$= \frac{1}{2}(1 + \cos 2\omega_c t) - \frac{1}{2}\sin(\omega_c + \omega_c)t - \frac{1}{2}\sin(\omega_c - \omega_c)t$$

$$\mathrm{Q} = \frac{1}{2} + \frac{1}{2}\underbrace{\cos 2\omega_c t}_{\text{(filtered out)}} - \frac{1}{2}\sin 2\omega_c t - \frac{1}{2}\underbrace{\sin 0}_{\text{(equals 0)}}$$

$$= \frac{1}{2}\mathrm{V} \text{(logic 1)}$$