## ARITHMETIC CIRCUITS

Arithmetic logic circuits are the logic circuits which perform arithmetic operations like addition, subtraction in digital computers.

Half adder: It is a combinational logic circuit which performs the addition of two bits resulting in two outputs - Sum and Carry.

## Block diagram of half adder



Logic diagram or logic circuit of half adder


## Truth table of half adder

| Inputs |  | Outputs |  |
| :---: | :---: | :---: | :---: |
| $\mathbf{A}$ | B | Sum = A $\oplus \mathbf{B}$ | Carry $=\mathbf{A B}$ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

## Timing Diagram



Half adder using universal NAND gates


Boolean expression:
Sum $=\mathbf{A} \oplus \mathbf{B}=\overline{\mathbf{A}} \mathbf{B}+\mathbf{A} \overline{\mathbf{B}}$
Carry $=\mathrm{AB}$
Full adder: It is a combinational logic circuit which performs the addition of three bits resulting in two outputs - Sum and Carry.

## Block diagram of full adder



Truth table of full adder

| Inputs |  |  | Outputs |  |
| :---: | :---: | :---: | :---: | :---: |
| A | B | C | Sum $=\mathrm{A} \oplus \mathrm{BQ} \mathrm{C}$ | Carry $=\mathrm{AB}+\mathrm{BC}+\mathrm{CA}$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## Logic circuit of full adder



Boolean expression for the sum
Sum $==A+B+C$
Sum $=\bar{A} \bar{B} C+\bar{A} B \bar{C}+A B \bar{C}+A B C$

Boolean expression for the carry

$$
\text { Carry }=A B+B C+A C
$$

Timing Diagram


Half Subtractor: It is combinational logic circuits which performs the subtraction of two bits resulting in two outputs - Difference and Borrow.

Block diagram of half Subtractor


Logic diagram or logic circuit of half ubtractor


## Truth table of half Subtractor

| Inputs |  | Outputs |  |
| :---: | :---: | :---: | :---: |
| A | B | Difference $=\mathrm{A} \oplus \mathrm{B}$ | Borrow $=\overline{\mathrm{A}} \mathrm{B}$ |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

Boolean expression:
Difference $=\mathbf{A} \Phi \mathbf{B}=\overline{\mathbf{A}} \mathbf{B}+\mathbf{A} \overline{\mathbf{B}}$
Borrow $=\overline{\mathbf{A}} \mathbf{B}$

Half subtractor using universal NAND gates



Full subtractor: It is combinational logic circuits which performs the subtraction of three bits resulting in two outputs difference and borrow.

Block diagram of full Subtractor

Inputs


## Truth table of full subtractor

## Logic circuit of full subtractor

| Input |  |  | Output |  |
| :---: | :---: | :---: | :---: | :---: |
| A | B | C | Difference <br> $=\mathrm{A} \oplus \mathrm{B} \oplus \mathrm{C}$ | Borrow $\overline{\mathrm{A}} \mathrm{C}$ <br> $+\overline{\mathrm{A}} \mathrm{B}+\mathrm{B} \mathrm{C}$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |



## 4 BIT PARALLEL BINARY ADDER:

A Parallel Adder is a digital circuit capable of finding the arithmetic sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel. It consists of full adders connected in cascade where the output carry from each full adder is connected to the carry input of the next higher order full adder

Consider two 4-bit binary numbers $\mathrm{B}_{4} \mathrm{~B}{ }_{3} \mathrm{~B}{ }_{2} \mathrm{~B}{ }_{1}$ and $\mathrm{A}_{4} \mathrm{~A}_{3} \mathrm{~A}_{2} \mathrm{~A}_{1}$ are to be added with a carry input $\mathrm{C}_{1}$. This can be done by cascading four full adder circuits as shown in Figure. The least significant bits $\mathrm{A}_{1}, \mathrm{~B}_{1}$, and $\mathrm{C}_{1}$ are added to the produce sum output $\mathrm{S}_{1}$ and carry output $\mathrm{C}_{2}$. Carry output $\mathrm{C}_{2}$ is then added to the next significant bits $\mathrm{A}_{2}$ and $\mathrm{B}_{2}$ producing sum output $\mathrm{S}_{2}$ and carry output $\mathrm{C}_{3} . \mathrm{C}_{3}$ is then added to $\mathrm{A}_{3}$ and $\mathrm{B}_{3}$ and so on. Thus finally producing the four-bit sum output $S_{4} S_{3} S_{2} S_{1}$ and final carry output Cout.


## Magnitude Comparator

Data comparison is needed in digital systems while performing arithmetic or logical operations. This comparison determines whether one number is greater than, equal, or less than the other number.

A Magnitude Comparator is a combinational circuit that compares two binary numbers in order to find out whether one binary number is equal, less than or greater than the other binary number.

The Block diagram of Magnitude Comparator is as shown below.


## Types of Magnitude Comparator:

1. 1-bit magnitude comparator.
2. 2-bit magnitude comparator.
3. 3-bit magnitude comparator.
4. 4-bit magnitude comparator.

## 2-bit magnitude comparator:

A 2-bit comparator compares two binary numbers, each of two bits and produces their relation such as one number is equal or greater than or less than the other. The figure below shows the block diagram of a two-bit comparator which has four inputs and three outputs.

The first number A is designated as $\mathrm{A}=\mathrm{A} 1 \mathrm{~A} 0$ and the second number is designated as $\mathrm{B}=$ B 1 B 0 . This comparator produces three outputs as $\mathrm{G}(\mathrm{G}=1$ if $\mathrm{A}>\mathrm{B}), \mathrm{E}(\mathrm{E}=1$, if $\mathrm{A}=\mathrm{B})$ and $\mathrm{L}(\mathrm{L}=1$ if $A<B$ ).


The truth table for a 2-bit comparator is given below:

| Inputs |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{A}_{\mathbf{1}}$ | $\mathbf{A}_{0}$ | $\mathbf{B}_{\mathbf{1}}$ | $\mathbf{B}_{0}$ | $\mathbf{A}>\mathbf{B}$ | $\mathbf{A}=\mathbf{B}$ | $\mathbf{A}<\mathbf{B}$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 |

## 4-Bit Comparator

It can be used to compare two four-bit words. The two 4-bit numbers are $A=A_{3} A_{2} A_{1} A_{0}$ and $B_{3} B_{2} B_{1} B_{0}$ where $A_{3}$ and $B_{3}$ are the most significant bits.

It compares each of these bits in one number with bits in that of other number and produces one of the following outputs as $\mathrm{A}=\mathrm{B}, \mathrm{A}<\mathrm{B}$ and $\mathrm{A}>\mathrm{B}$.

The output logic statements of this converter are

- If $A 3=1$ and $B 3=0$, then $A$ is greater than $B(A>B)$. Or
- If A3 and B3 are equal, and if $\mathrm{A} 2=1$ and $\mathrm{B} 2=0$, then $\mathrm{A}>\mathrm{B}$. Or
- If A3 and B3 are equal \& A2 and B2 are equal, and if $\mathrm{A} 1=1$, and $\mathrm{B} 1=0$, then $\mathrm{A}>\mathrm{B}$. Or
- If A3 and B3 are equal, A2 and B2 are equal and A1 and B1 are equal, and if A0 $=1$ and B0 $=0$, then $\mathrm{A}>\mathrm{B}$.


## Block diagram:



## Truth table

| COMPARING INPUTS |  |  |  | OUTPUT |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A $>$ B | A<B | A $=$ B |
| A3 > B3 | X | X | X | H | L | L |
| A3 < B3 | X | X | X | L | H | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2>\mathrm{B} 2$ | X | X | H | L | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2<\mathrm{B} 2$ | X | X | L | H | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | A1 > B1 | X | H | L | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{Al}<\mathrm{B} 1$ | X | L | H | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{Al}=\mathrm{B} 1$ | A0 > B0 | H | L | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{Al}=\mathrm{B} 1$ | $\mathrm{A} 0<\mathrm{B} 0$ | L | H | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{Al}=\mathrm{B} 1$ | $\mathrm{A} 0=\mathrm{B} 0$ | H | L | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{Al}=\mathrm{B} 1$ | $\mathrm{A} 0=\mathrm{B} 0$ | L | H | L |
| $\mathrm{A} 3=\mathrm{B} 3$ | $\mathrm{A} 2=\mathrm{B} 2$ | $\mathrm{Al}=\mathrm{B} 1$ | $\mathrm{A} 0=\mathrm{B} 0$ | L | L | H |
| $\mathrm{H}=$ High Voltage Level, L = Low Voltage, Level, $\mathrm{X}=$ Don't Care |  |  |  |  |  |  |

## Reference Books:

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3. https://www.electronics-tutorials.ws/combination/comb 8.html
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